

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Application No.:

Patent No.:

Filed:

Issue Date:

Title:

Commissioner for Patents  
Washington, D.C. 20231

**POWER OF ATTORNEY BY ASSIGNEE OF ENTIRE INTEREST**  
**(REVOCATION OF PRIOR POWERS)**

As assignee of record of each of the patents listed in the table of attachment A,

**REVOCATION OF PRIOR POWERS OF ATTORNEY**

all powers of attorney previously given in each of the listed patents are hereby revoked, and

**NEW POWER OF ATTORNEY**

the following attorneys/agents are hereby appointed to prosecute this patent/application and to transact all business in the Patent and Trademark Office connected therewith: I hereby appoint all attorneys of Thomas, Kayden, Horstemeyer & Risley, LLP, who are listed under the USPTO Customer Number shown below as the attorneys to prosecute this patent/application and to transact all business in the United States Patent and Trademark Office connected therewith, recognizing that the specific attorneys listed under that Customer Number may be changed from time to time at the sole discretion of Thomas, Kayden, Horstemeyer & Risley, LLP, and request that all correspondence about the application be addressed to the address filed under the same USPTO Customer Number:

**15650**

Patent Trademark Office

Please direct all future correspondence and telephone calls to:

**Scott A. Horstemeyer, Reg. No. 34,183**  
**THOMAS, KAYDEN, HORSTEMEYER & RISLEY, L.L.P.**  
400 Interstate North Parkway  
Atlanta, Georgia 30339  
770-933-9500

**ASSIGNEE OF ENTIRE INTEREST**

**BROADCOM CORPORATION**

5300 California Avenue  
Irvine, California 92617-3038

**ASSIGNEE CERTIFICATION**

The certification under 37 C.F.R. §3.73(b) establishing the right of assignee to take action is attached hereto along with documentation evidencing same. Further, in my official position with Broadcom Corporation, I am authorized to sign documents and otherwise act on its behalf in connection with the management and handling of patent applications and other intellectual property matters.

Date: 9/12/11

  
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**Dee Henderson**  
Director - Intellectual Property Administration  
Broadcom Corporation

## ATTACHMENT A

No.	Patent No.	BD No.	Patent Title	Issue Date	Assignment to BD (Reel/Frame)
1	7,848,430	BU1233.1C2	VIDEO AND GRAPHICS SYSTEM WITH AN MPEG VIDEO DECODER FOR CONCURRENT MULTI-ROW DECODING	12/7/2010	011581/0971
2	6,738,072	BU1265	GRAPHICS DISPLAY SYSTEM WITH ANTI-FLUTTER FILTERING AND VERTICAL SCALING FEATURE	5/18/2004	010709/0730
3	7,554,553	BU1265C4	GRAPHICS DISPLAY SYSTEM WITH ANTI-FLUTTER FILTERING AND VERTICAL SCALING FEATURE	6/30/2009	010709/0730
4	6,380,945	BU1204	GRAPHICS DISPLAY SYSTEM WITH COLOR LOOK-UP TABLE LOADING MECHANISM	4/30/2002	010697/0074
5	6,774,472	BU1209	GRAPHICS DISPLAY SYSTEM WITH VIDEO SYNCHRONIZATION FEATURE	6/1/2004	011185/0189
6	7,446,774	BU1233.8	VIDEO AND GRAPHICS SYSTEM WITH AN INTEGRATED SYSTEM BRIDGE CONTROLLER	11/4/2008	011583/0685
7	7,098,930	BU1265C2	GRAPHICS DISPLAY SYSTEM WITH ANTI-FLUTTER FILTERING AND VERTICAL SCALING FEATURE	8/29/2006	010709/0730
8	7,554,562	BU1265C5	GRAPHICS DISPLAY SYSTEM WITH ANTI-FLUTTER FILTERING AND VERTICAL SCALING FEATURE	6/30/2009	010709/0730
9	7,440,030	BU2061	METHOD AND APPARATUS FOR INTERLACED DISPLAY OF PROGRESSIVE VIDEO CONTENT	10/21/2008	013424/0672

No.	Patent No.	BD No.	Patent Title	Issue Date	Assignment to BD (Reel/Frame)
10	7,310,104	BU1265C3	GRAPHICS DISPLAY SYSTEM WITH ANTI-FLUTTER FILTERING AND VERTICAL SCALING FEATURE	12/18/2007	010709/0730
11	6,879,330	BU1265C1	GRAPHICS DISPLAY SYSTEM WITH ANTI-FLUTTER FILTERING AND VERTICAL SCALING FEATURE	4/12/2005	010709/0730
12	6,721,837	BU1266C2	GRAPHICS DISPLAY SYSTEM WITH UNIFIED MEMORY ARCHITECTURE	4/13/2004	010689/0710
13	7,082,143	BU1357.2	VOICE AND DATA EXCHANGE OVER A PACKET BASED NETWORK WITH DTMF	7/25/2006	011825/0878
14	6,819,330	BU1204C1	GRAPHICS DISPLAY SYSTEM WITH COLOR LOOK-UP TABLE LOADING MECHANISM	11/16/2004	022416/0511
15	7,015,928	BU1204C2	GRAPHICS DISPLAY SYSTEM WITH COLOR LOOK-UP TABLE LOADING MECHANISM	3/21/2006	022416/0511
16	6,529,935	BU1266C1	GRAPHICS DISPLAY SYSTEM WITH UNIFIED MEMORY ARCHITECTURE	3/4/2003	010689/0710
17	7,423,983	BU1357	VOICE AND DATA EXCHANGE OVER A PACKET BASED NETWORK	9/9/2008	010947/0095
18	7,911,483	BU1206	GRAPHICS DISPLAY SYSTEM WITH WINDOW SOFT HORIZONTAL SCROLLING MECHANISM	3/22/2011	012151/0894
19	7,773,741	BU1300	VOICE AND DATA EXCHANGE OVER A PACKET BASED	8/10/2010	011046/0666

No.	Patent No.	BD No.	Patent Title	Issue Date	Assignment to BD (Reel/Frame)
			NETWORK WITH ECHO CANCELLATION		
20	7,161,931	BU1358	VOICE AND DATA EXCHANGE OVER A PACKET BASED NETWORK	1/9/2007	010964/0645
21	7,062,595	BU1900	INTEGRATED GIGABIT ETHERNET PCI-X CONTROLLER	6/13/2006	015735/0148
22	7,180,892	BU1333	VOICE AND DATA EXCHANGE OVER A PACKET BASED NETWORK WITH VOICE DETECTION	2/20/2007	011843/0946
23	7,653,536	BU133C1	VOICE AND DATA EXCHANGE OVER A PACKET BASED NETWORK WITH VOICE DETECTION	1/26/2010	011843/0946
24	7,933,227	BU1357C1	VOICE AND DATA EXCHANGE OVER A PACKET BASED NETWORK	4/26/2011	021476/0715
25	7,451,335	BU1900.2	SELECTIVELY DISABLING A PORTION OF ASF OPERATIONS WHEN ASF DEVICE IS POWERED BY AUXILIARY POWER	11/11/2008	013105/0162

No.	Patent No.	BD No.	Patent Title	Issue Date	Assignment to BD (Reel/Frame)
26	7,684,330	BU2021C1	FLOW BASED CONGESTION CONTROL	3/23/2010	013022/0227
27	7,132,963	BU20793	METHODS AND APPARATUS FOR PROCESSING VARIABLE LENGTH CODED DATA		022083/0433
28	7,194,047	BU20794	RECEIVER FOR ROBUST DATA EXTENSION FOR 8VSB SIGNALING	3/20/2007	022083/0433
29	7,253,818	BU20795	SYSTEM FOR TESTING MULTIPLE DEVICES ON A SINGLE SYSTEM AND METHOD THEREOF	8/7/2007	022083/0433
30	7,697,903	BU5917	METHOD AND SYSTEM FOR LEVEL DETECTOR CALIBRATION FOR ACCURATE TRANSMIT POWER CONTROL	4/13/2010	018886/0572
31	7,729,671	BU5918	METHOD AND SYSTEM FOR ENHANCING EFFICIENCY BY MODULATING POWER AMPLIFIER GAIN	6/1/2010	019551/0940
32	7,538,610	BU5919	METHOD AND SYSTEM FOR ENHANCEMENT OF POWER AMPLIFIER EFFICIENCY THROUGH CONTROLLED VARIATION OF GAIN IN A POWER AMPLIFIER DRIVER	5/26/2009	018941/0428
33	7,436,253	BU5922	METHOD AND SYSTEM FOR FAST CALIBRATION TO CANCEL PHASE FEEDTHROUGH	10/14/2008	019177/0988
34	7,809,408	BU5924	METHOD AND SYSTEM FOR A POWER SWITCH WITH A SLOW IN-RUSH CURRENT	10/5/2010	019636/0521

No.	Patent No.	BD No.	Patent Title	Issue Date	Assignment to BD (Reel/Frame)
35	7,616,069	BU5898	METHOD AND SYSTEM FOR FAST PLL CLOSE- LOOP SETTLING AFTER OPEN-LOOP VCO CALIBRATION	11/10/2009	018931/0892
36	7,825,738	BU5899	METHOD AND SYSTEM FOR IMPLEMENTING A LOW POWER, HIGH PERFORMANCE FRACTIONAL-N PLL	11/2/2010	019692/0572